EE8351 DIGITAL LOGIC CIRCUITS L T P C

UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES 6+6

Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code) - Digital Logic Families -comparison of RTL, DTL, TTL, ECL and MOS families -operation, characteristics of digital logic family.

UNIT II COMBINATIONAL CIRCUITS 6+6

Combinational logic - representation of logic functions-SOP and POS forms, K-map representations - minimization using K maps - simplification and implementation of combinational logic – multiplexers and de multiplexers - code converters, adders, subtractors, Encoders and Decoders.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS 6+6

Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits – Moore and Melay models- Counters, state diagram; state reduction; state assignment.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES 6+6

Asynchronous sequential logic circuits-Transition tability, flow tability-race conditions,

hazards &errors in digital circuits; analysis of asynchronous sequential logic circuitsintroduction to Programmability Logic Devices: PROM – PLA –PAL, CPLD-FPGA.

UNIT V VHDL 6+6

RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages – Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).

TOTAL : 60 PERIODS